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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,399	10/07/2003	Sheng-Hua Chen	TOP 336	5475

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EXAMINER	
NGUYEN, JOHN B	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Applicati n No.	Applicant(s)	
	10/679,399	CHEN ET AL.	
	Examiner	Art Unit	
	John B Nguyen	2819	

-- The MAILING DATE of this communication appears n the cover sheet with the corresp ndence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 6 is/are allowed.

6)☒ Claim(s) 1-4 is/are rejected.

7)☒ Claim(s) 5 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 10/07/2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 5, line 14, the term "a fourth NMOS transistor ..." is objected to because of the following informalities: a fourth NMOS transistor were previously recited in claim 4, lines 2 and 3. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaminaga et al (US Patent No. 5,880,602).

Regarding to claim 1, Fig. 9 Kaminaga et al. disclose an I/O buffer driven by a system voltage, comprising: an input/output circuit (transistors QP3, QN3) comprising a first PMOS transistor (QP3) and a first NMOS transistor (QN3) and having an I/O port (drain of QN3 and QP3) coupled to an I/O pad (PAD), wherein the first PMOS transistor has an N-well region (QP3, dark arrow), a gate of the first NMOS transistor receives a first gate control signal (output from Q2

connected to the gate of QN3), and a drain of the first PMOS transistor serves as the I/O port (drain of QP3 connected to I/O PAD);

a N-well control circuit (includes transistors QP5, QN11, QP21, QP53, QN12, Q5) coupled to I/O pad (PAD) to control the voltage level at the N-well region of the first PMOS transistor (column 9, lines 26-45); and

a P-gate control circuit (transistors QP2, QP1, QN1) receiving a second gate control signal (output from Q1 connected to the QN1 and QP1) and being output to the gate of the first PMOS transistor (output of QN1 and QP1 connected to the gate of QP3), wherein the P-gate control circuit (transistors QP2, QP1, QN1) comprises: a transmission gate (QN1 and QP1) having a second NMOS transistor (QN1) and a second PMOS transistor (QP1), the sources of which are coupled to the second gate control signal (output from Q1 connected to source of QN1 and QP1), and the gates of which are coupled to the system voltage (the gate of QN1 connected to Vcc1) and the N-well control circuit respectively (P-gate and N-well control circuits are coupled); and

a third PMOS transistor (QP2) having a drain and a source coupled to the gate and the floating N-well region of the first PMOS transistor respectively (QP2 and QP3 are coupled respectively), and a gate coupled to the system voltage (the gate of QP2 is connected to Vcc1).

4. Regarding to claim 2, wherein the N-well control circuit adjusts the voltage level at the N-well region of the first PMOS transistor to the voltage level of the input voltage when the input voltage exceeds the system voltage (ABSTRACT).

5. Regarding to claim 3, wherein the N-well control circuit the voltage level at the N-well region of the first PMOS transistor to the voltage level of the system voltage when the input voltage is lower than the system voltage (ABSTRACT).

6. Regarding to claim 4, wherein the input/output circuit further comprises a fourth NMOS transistor (QN2) having a source and drain coupled to the I/O pad (PAD) and the drain of the first NMOS transistor respectively (source QN2 connected to drain QN3), and a gate coupled to the system voltage (gate QN2 connected to Vcc1).

Allowable Subject Matter

7. Claim 6 is allowed.

8. The following is an examiner's statement of reasons for allowance:

The prior art fails to teach or fairly suggest an input/output buffer, comprising: a third PMOS transistor having a drain coupled to a source of the third NMOS transistor. Therefore, claim 6 is allowed.

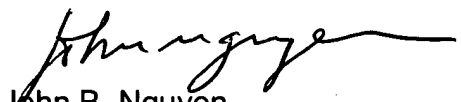
9. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. (See enclosed Form PTO-892).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B Nguyen whose telephone number (571) 272-1808. The examiner can normally be reached on 8AM-4: 30 PM M-F.



John B. Nguyen
June 29, 2004